

FIG 1

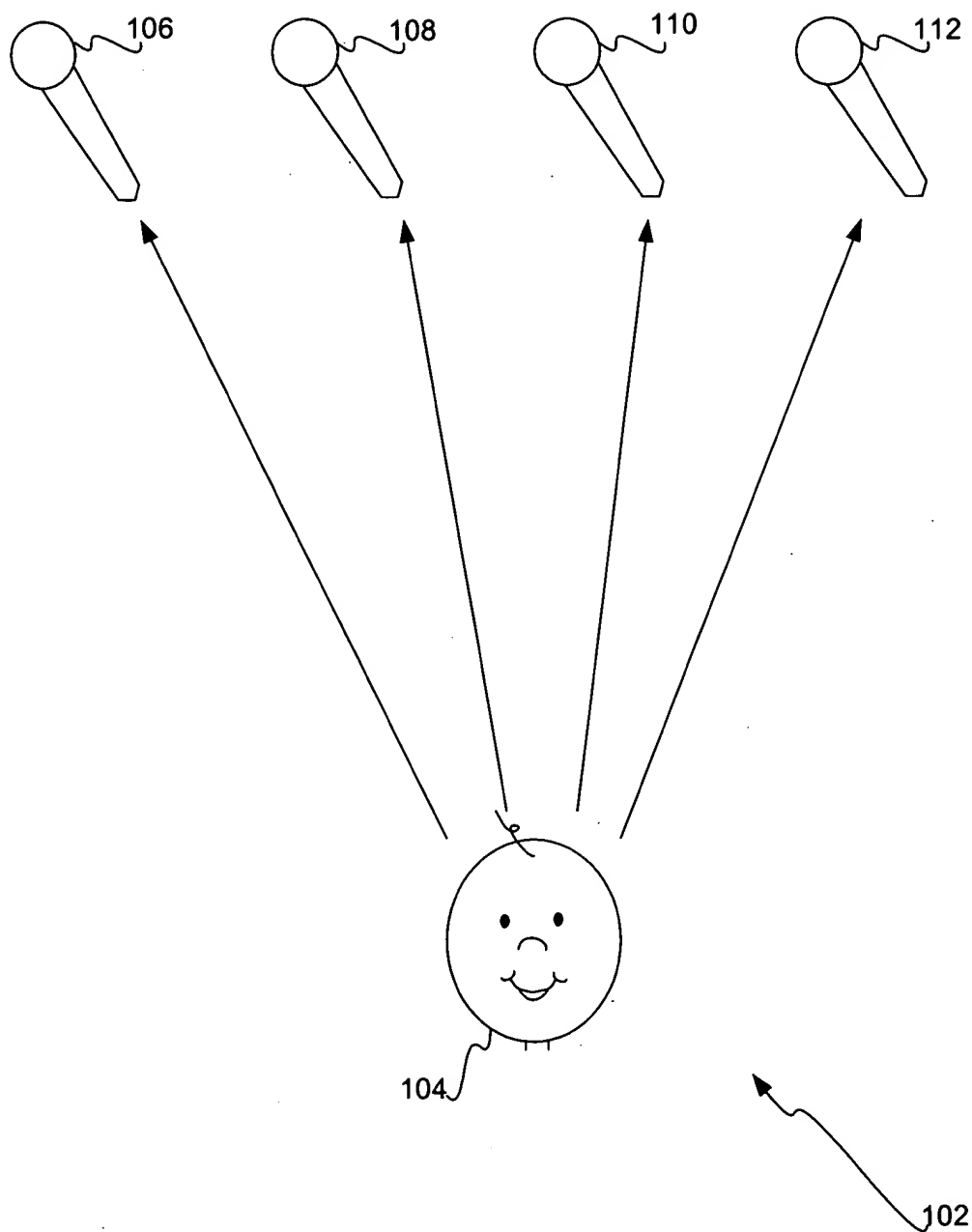


FIG 2

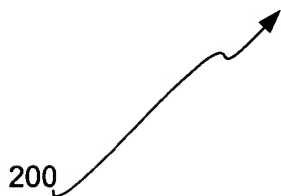
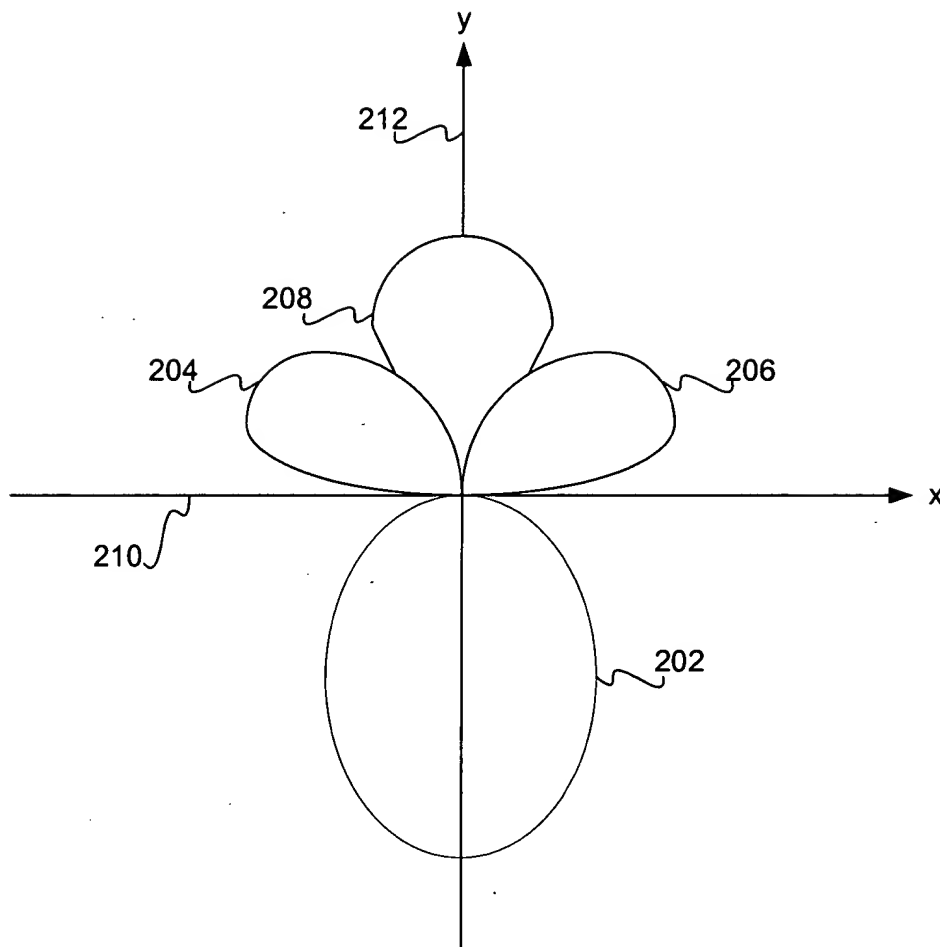


FIG 3

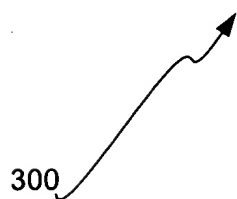
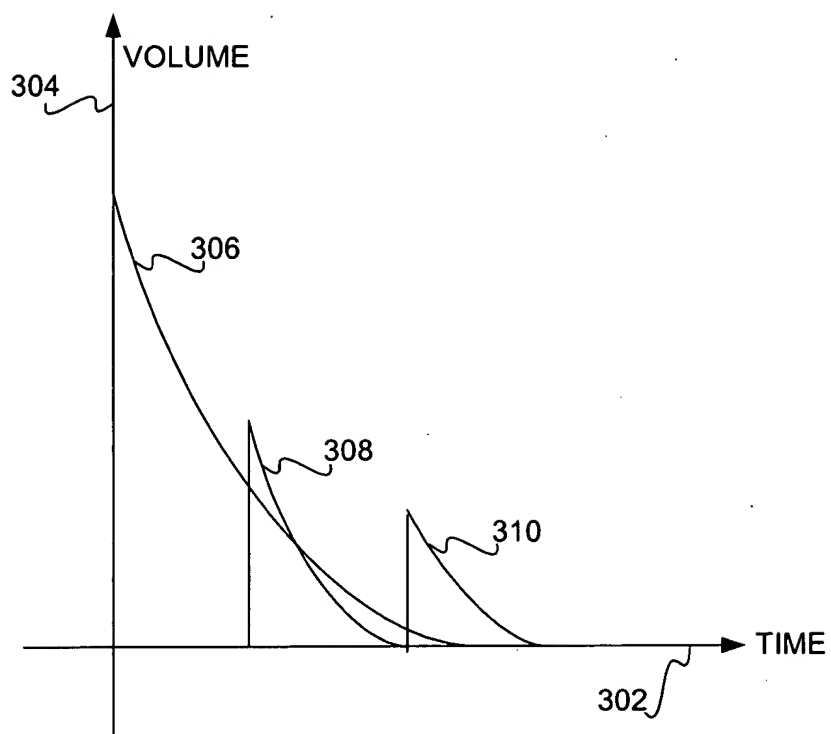


FIG 4

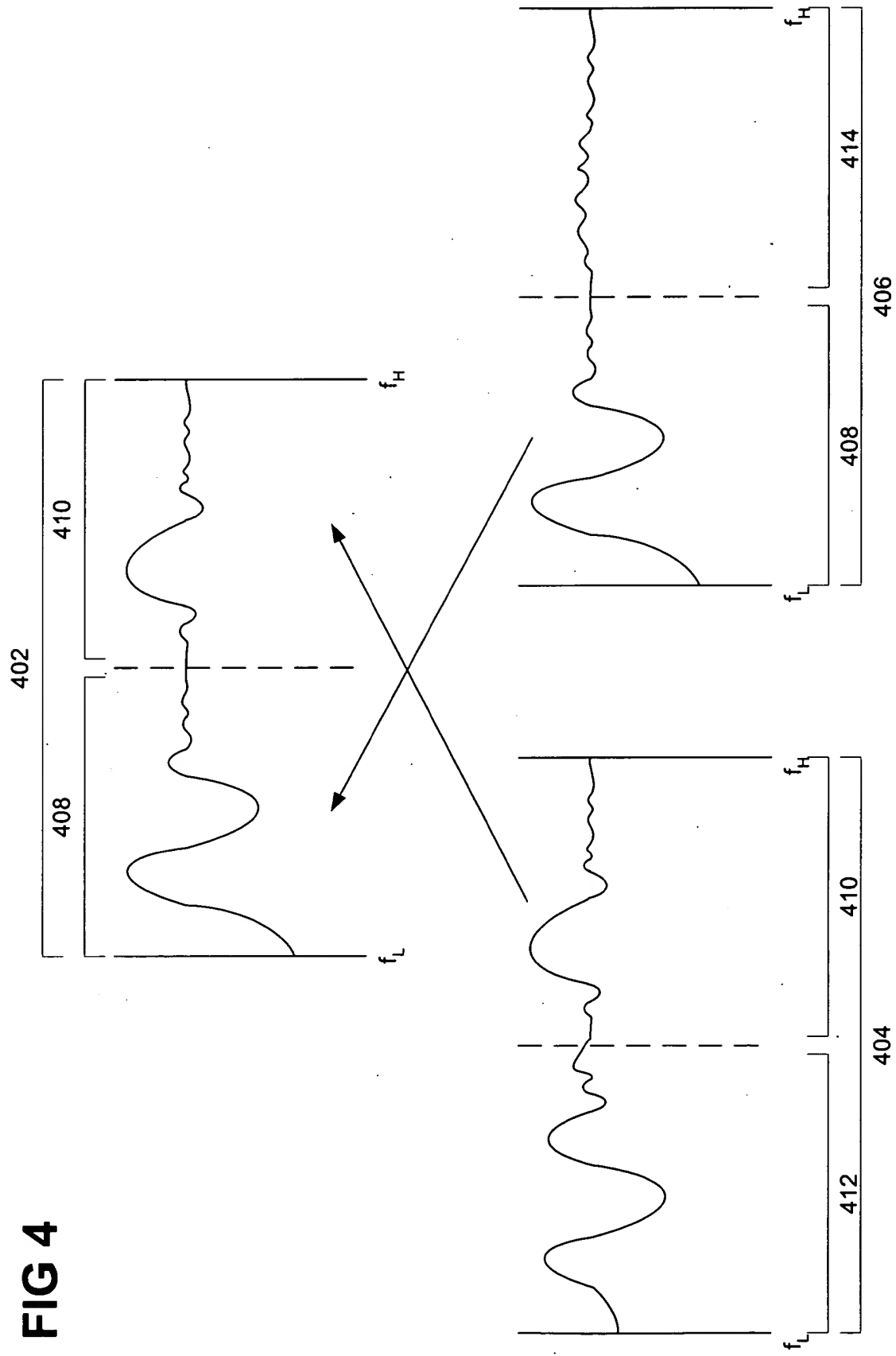


FIG 5

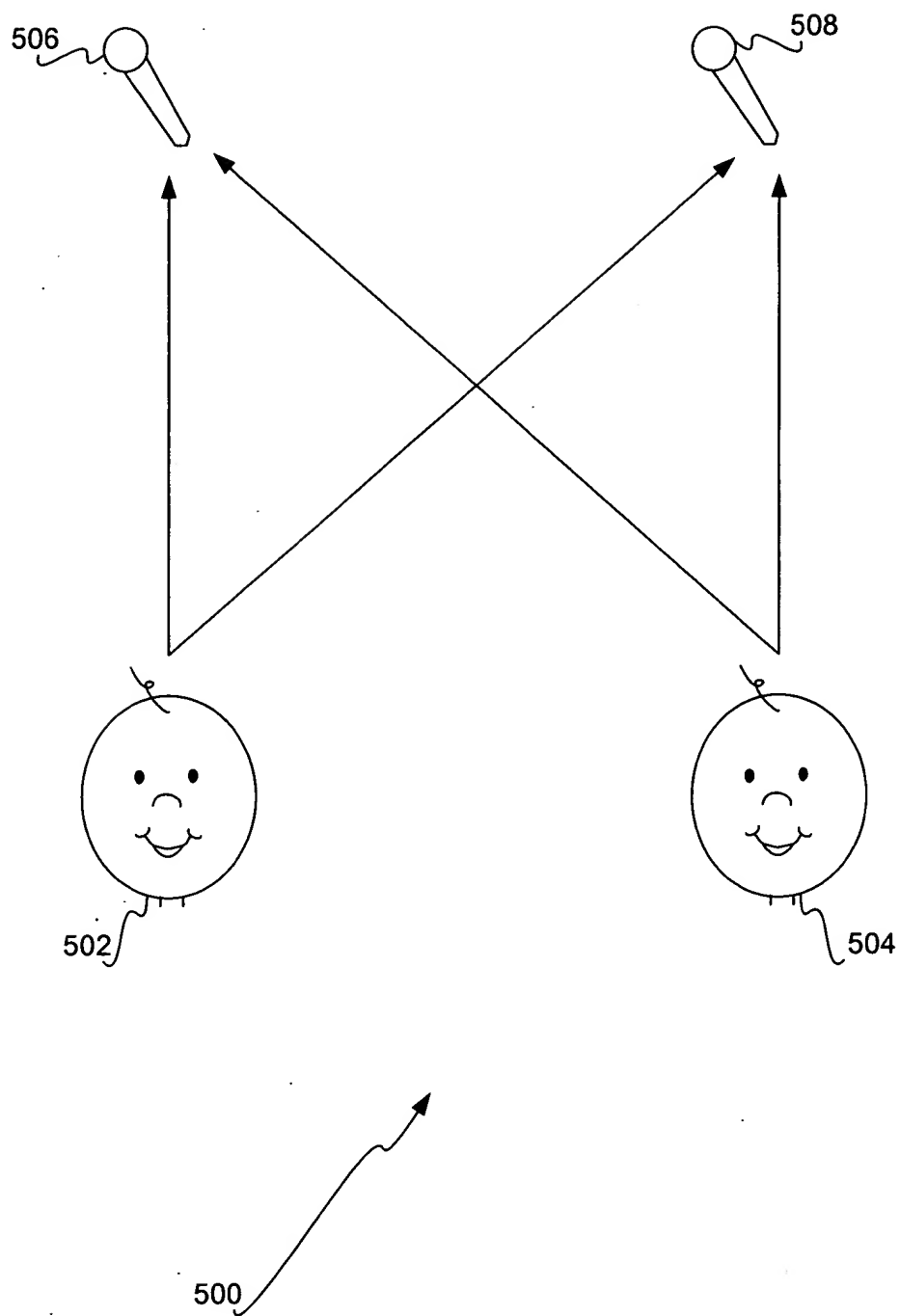


FIG 6

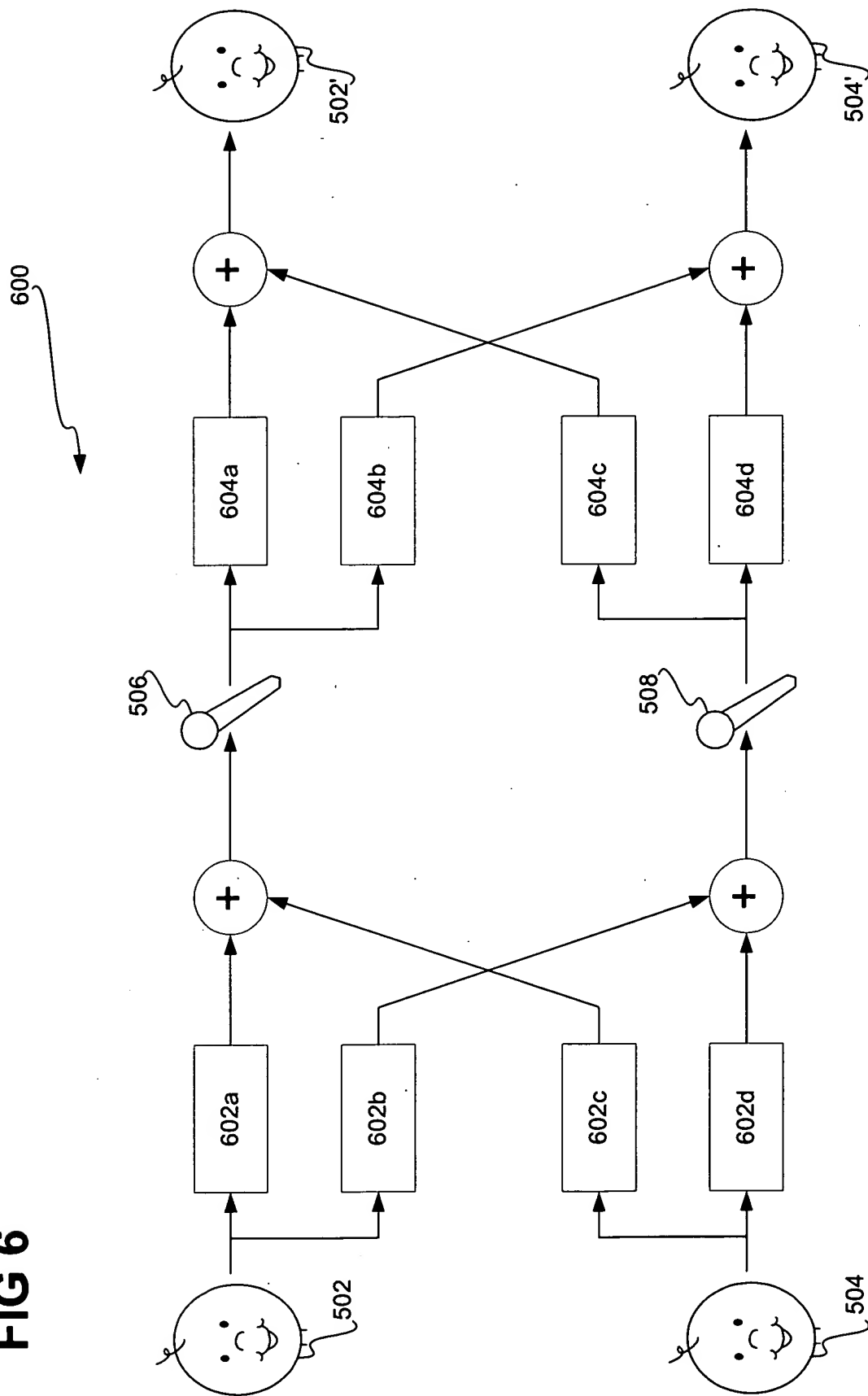


FIG 7

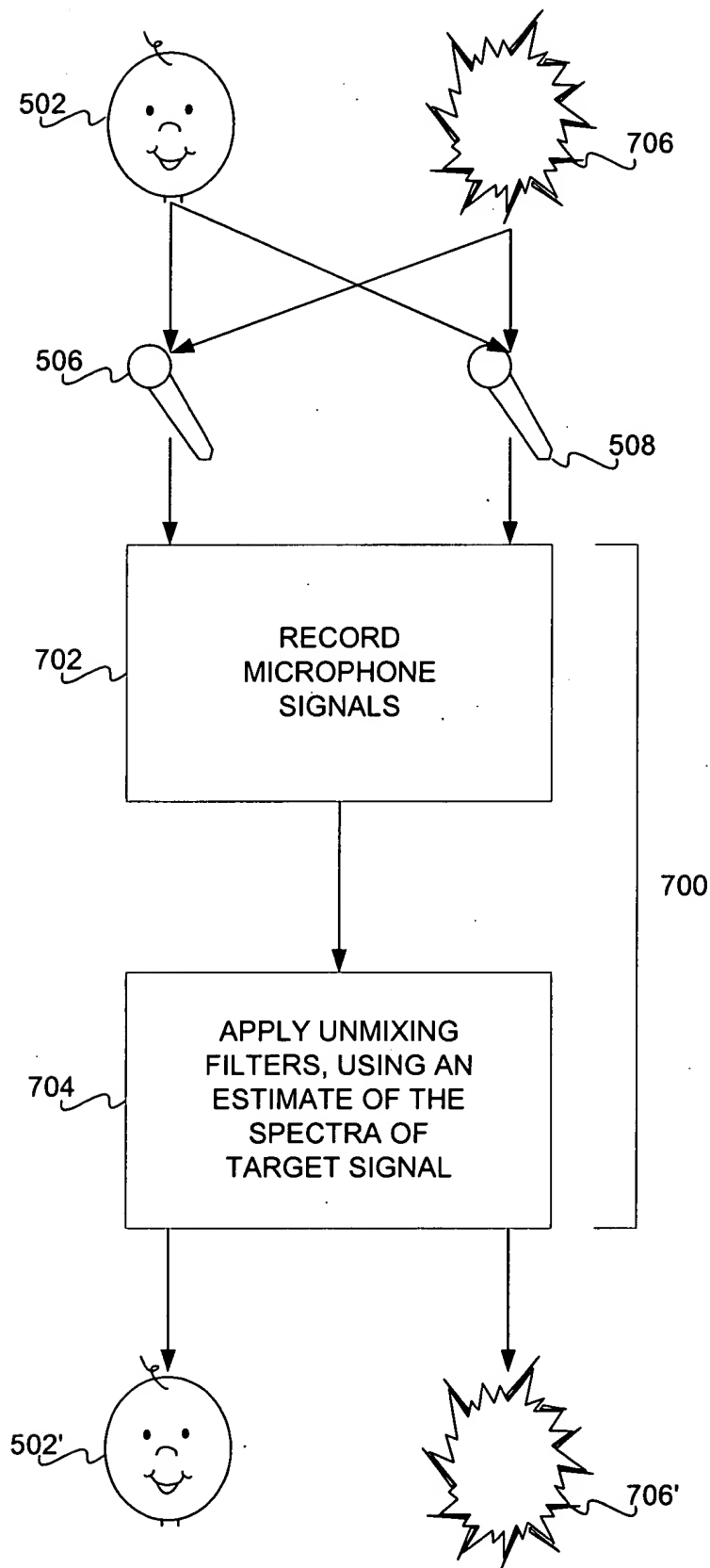
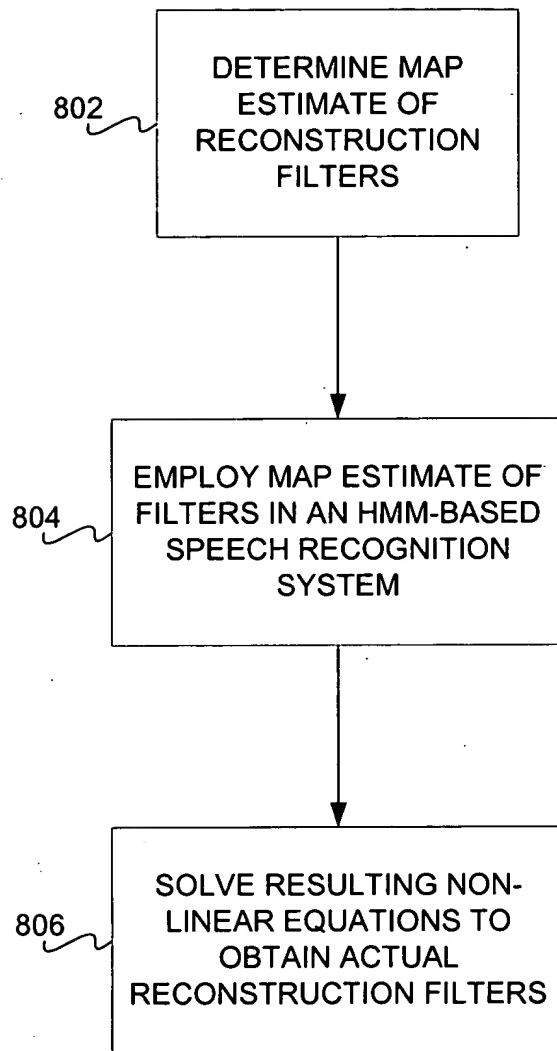
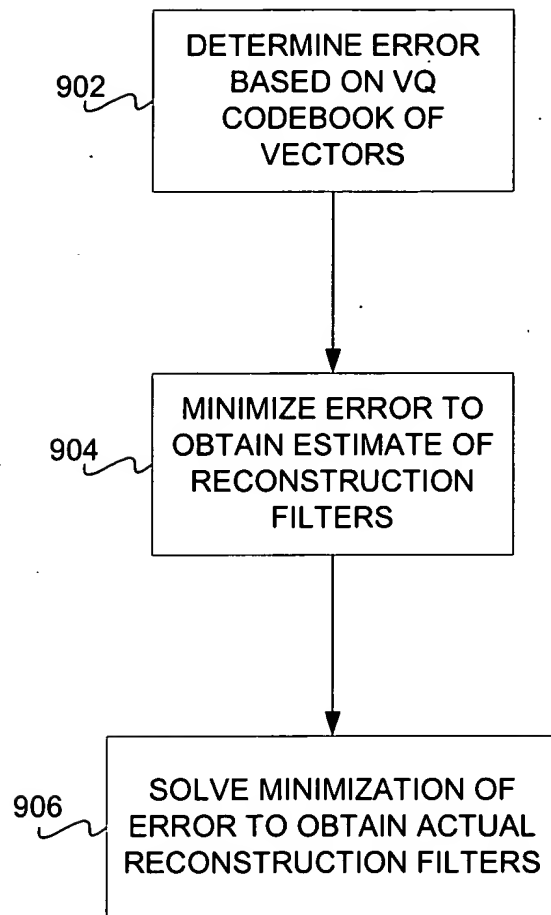


FIG 8



800

FIG 9



900

FIG 10

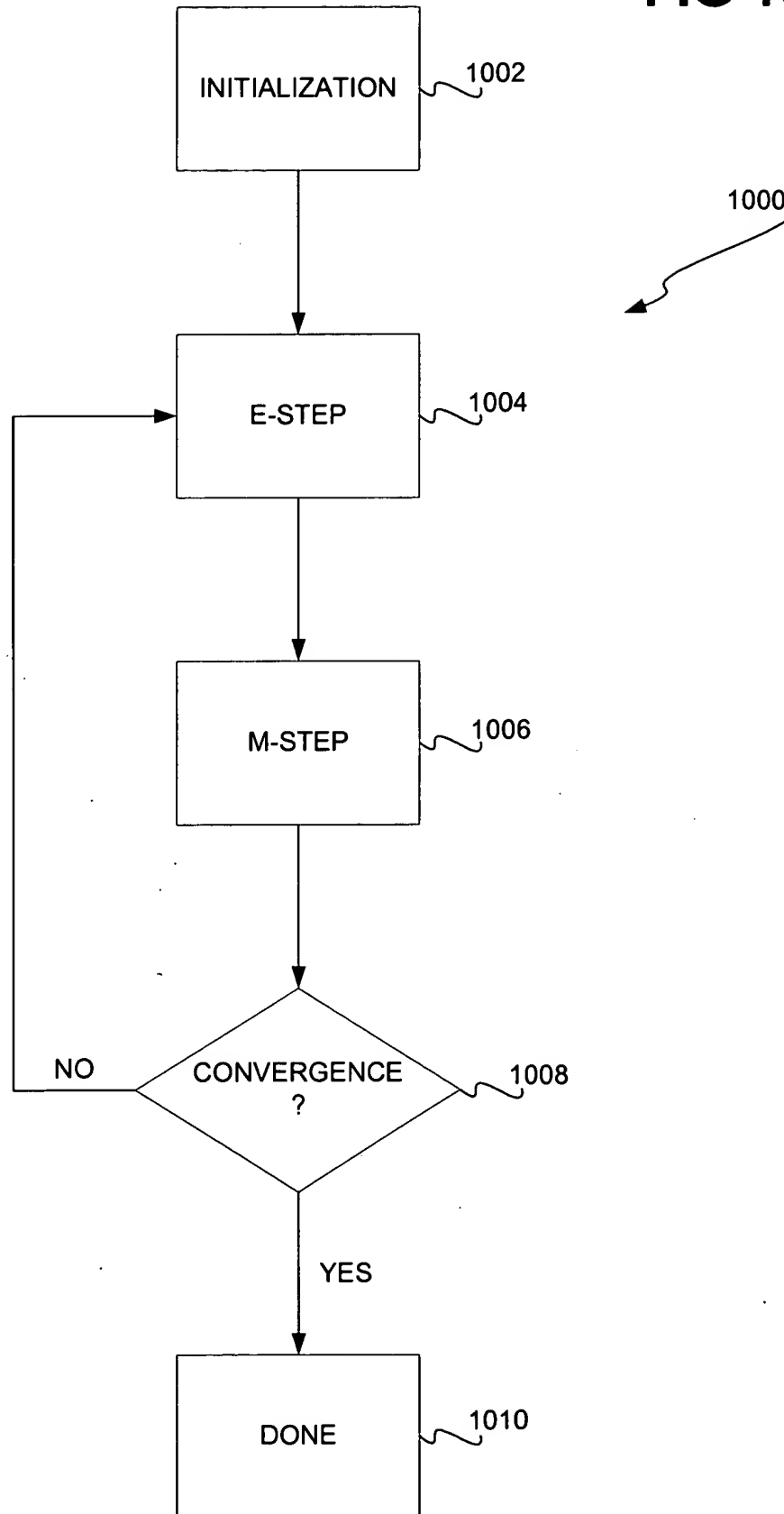


FIG. 11 is a block diagram of a system 10. The system 10 includes a processing unit 12, system memory 14, and communication connection(s) 22. The system memory 14 is divided into volatile and non-volatile sections. The system 10 also includes removable storage 18, non-removable storage 20, output device(s) 26, and input device(s) 24.

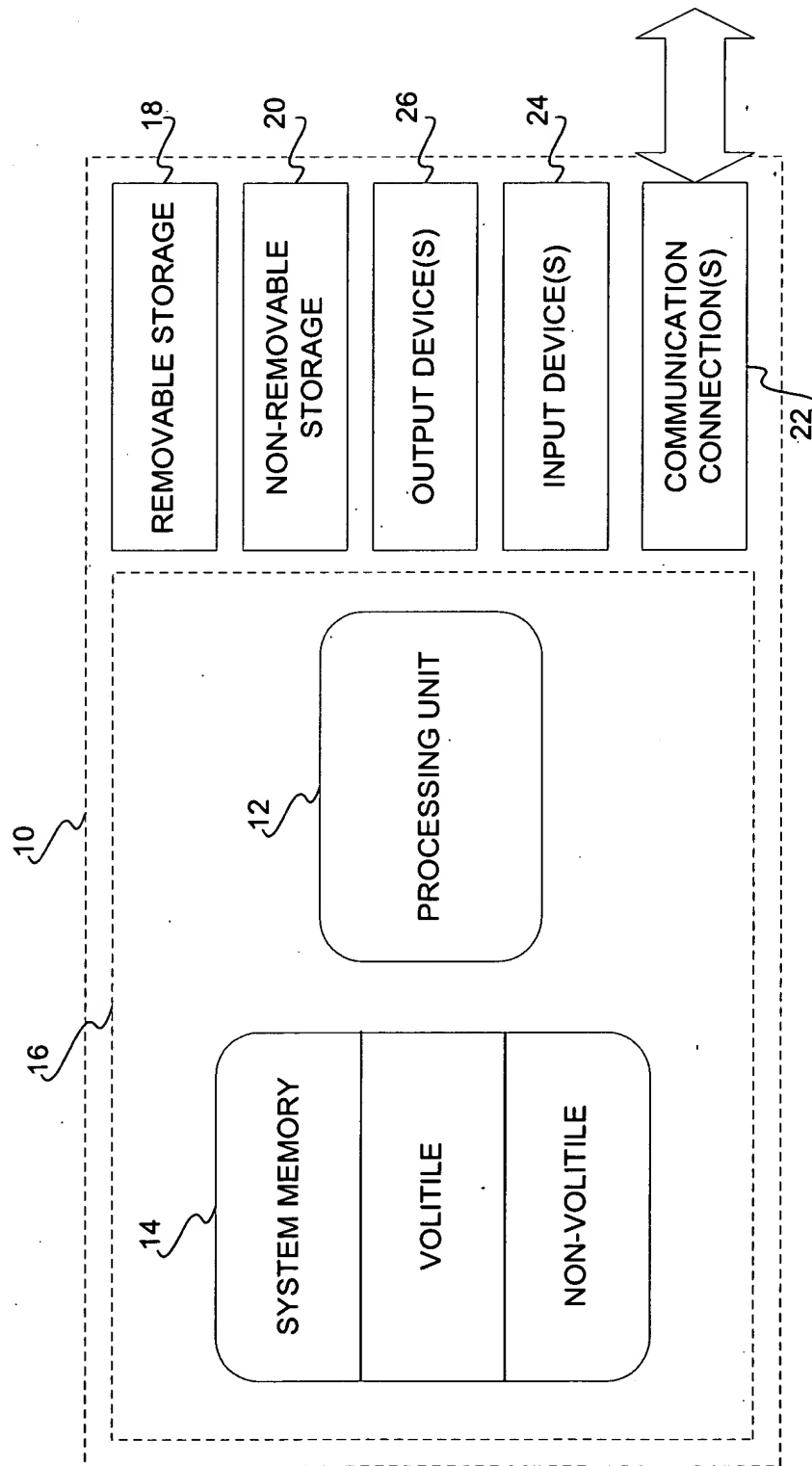


FIG 11